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IN THE CLAIMS

The listing of claims will replace all prior versions, and listing, of claims in the application:

Claim 1 (currently amended): An amplifier circuit, comprising: an operational amplifier having a ~~non-converting first~~ input terminal coupled to a ~~ground common node~~, a ~~converting second~~ input terminal, and an output terminal;

a capacitive device coupled between the second input terminal and an input voltage; and
a resistor network comprising a plurality of stages connected serially, coupled between the ~~converting second~~ input terminal and the output terminal, wherein each stage of the resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the ~~ground common node~~; and

a second resistor coupled between the input node and the output node.

Claim 2 (currently amended): The amplifier circuit as claimed in claim 1, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 3 (currently amended): The amplifier circuit as claimed in claim 2, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R .

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Claim 4 (currently amended): An amplifier circuit, comprising:

an operational amplifier having a ~~non-converting~~ first input terminal coupled to a ground common node, a ~~converting~~ second input terminal, and an output terminal;

a first resistor network comprising a plurality of stages connected serially, coupled to the ~~converting~~ second input terminal for receiving an input voltage, wherein each stage of the first resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the ground common node; and

a second resistor coupled between the input node and the output node; and

a loading unit coupled between the ~~converting~~ second input terminal and the output terminal.

Claim 5 (currently amended): The amplifier circuit as claimed in claim 4, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 6 (currently amended): The amplifier circuit as claimed in claim 5, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R .

Claim 7 (currently amended): The amplifier circuit as claimed in claim 4, wherein the loading unit is a second resistor network comprising a plurality of stages connected serially, wherein each stage of the first resistor network comprises an input node, an output node, a third

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resistor coupled between the input node and the ground common node, and a fourth resistor coupled between the input node and the output node.

Claim 8 (currently amended): The amplifier circuit as claimed in claim 7, wherein the resistance of the third resistor is approximately two times larger than the resistance of the fourth resistor.

Claim 9 (currently amended): The amplifier circuit as claimed in claim 8, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the fourth resistor is R .

Claim 10 (currently amended): ~~A resistor network includes~~
~~— a plurality of stages connected serially, wherein each stage of the first resistor network comprises:~~
~~— an input node;~~
~~— an output node;~~
~~— a first resistor coupled between the input node and the ground; and~~
~~— a second resistor coupled between the input node and the output node, wherein the resistor network is implemented inside of an IC device~~ The amplifier circuit as claimed in claim 4, wherein the loading unit comprises a capacitive device.

Claim 11 (currently amended): The amplifier circuit as claimed in claim ~~10~~ 4, wherein the resistance of the first resistor is two times larger than the resistance of the second resistor loading unit comprises a resistor device.

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Claim 12 (currently amended): The amplifier circuit as claimed in claim 11, wherein the equivalent resistance of the resistor network is $2^n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R , resistor device comprises a second resistor network.

Claim 13 (currently amended): The amplifier circuit as claimed in claim 10, wherein each of the first resistor and the second resistor is implemented by a MOS transistor further comprising a capacitive device coupled between the first resistor network and the input voltage.

Claim 14 (new): An amplifier circuit, comprising:
an operational amplifier having a first input terminal coupled to a common node, a second input terminal, and an output terminal;
a capacitive device coupled between the second input terminal and the output terminal;
and

a resistor network comprising a plurality of stages connected serially, coupled between the second input terminal and the output terminal, wherein each stage of the resistor network comprises:

- an input node;
- an output node;
- a first resistor coupled between the input node and the common node; and
- a second resistor coupled between the input node and the output node.

Claim 15 (new): The amplifier circuit as claimed in claim 14, wherein the second input terminal is coupled to an input voltage.

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Claim 16 (new): The amplifier circuit as claimed in claim 14, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 17 (new): The amplifier circuit as claimed in claim 16, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R .

Claim 18 (new): The amplifier circuit as claimed in claim 14, further comprising a loading unit coupled between the second input terminal and an input voltage.

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